The VHDL file ‘project\_4’ is the design source file. The file ‘testbench’ is used for simulation. The XDC file ‘nexys 4DDR’ is the constrains file.

The button ‘B1’ is BTNL, the button ‘B2’ is BTNR, the button ‘B3’ is BTNC.

The verify birthday number is 0416 (0000 0100 0001 0110). The old passcode is 3469 (0011 0100 0110 1001).

The design could start with ‘verify\_reset’ part, and then the input part if the user press ‘B3’ at first, or just start with ‘input’ part if the user press ‘B1’ at first.

For the verify\_reset part, if ‘B3’ is pressed, LEDS= "1010101010" which could help the user know the ‘B3’ has been pressed, and the user could carry on the following functions. The user input the verify digit by using the switches on the FPGA board, the digit should be converted from decimal to binary, and input the binary digit by using the switches, and the 7-segments could display the input number in decimal formal. Pressing the button ‘B2’ after setting digit by SWITCHES.

If the LEDS=’ 1100000011’, it means the birthday number is wrong, the user have to reset the birthday number. If the LEDS =’ 0000110000’, the user should then set the length of the new passcode and press the ‘B2’. PLEASE NOTE THAT if the user want to reset the length of the new passcode is 7, the SWITCHES should be ‘0110’ (6), because the SWITCHES start from 0.

When the user has already set all the new passcode, the LEDS =’0000000001’ which means the reset process is finished.

With the help of SWITCHES, LEDS, DIGITS and button ‘B2’, the user could input the passcode, and open the lock.